INTERMODULATION DISTORTION IN GaAs FETs

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ABSTRACT

The influence that the active layer profile plays in determining the Intermodulation Distortion levels (IMD) in a power GaAs FET has been analyzed. A simplified model of a tuned amplifier containing the device sources of nonlinearity has yielded an improved understanding of generation of IMD products in such applications as GaAs FET power amplifiers.

Introduction

The GaAs FET has developed rapidly to a point of maturity at which it is employed in power amplifiers from 4 to 15 GHz. Because of the demand for greater output power, there is a need to know more about the mechanisms of how power output of the applied signals saturates and how power is diverted to the unwanted signals generated by nonlinearities in the device. Previous analyses have discussed such features of Intermodulation Distortion (IMD) as the dependence on input signal level and upon circuit tuning conditions. Kouno et. al.[1] in their analysis of third-order products have outlined a general method of calculation of intermodulation behavior. Their approach assigns a device several possible sources of nonlinearity and obtains from measurements a power series description of each nonlinearity source. In the present discussion new insights are provided by obtaining theoretical power series coefficients from modeling active layer profiles. Predictions are obtained of the effects that active layer profile will have on saturation and distortion using a model similar to that of Tucker and Rauscher.[2]

Sources of Nonlinear Distortion

The following analysis will consider input signal power levels at which the intermodulation products (IMD) are still defined as low power w.r.t. the signal level and where there is still useful gain although more than 1 dB below the small signal level. In Figure 1 the case (c) represents the I-V characteristic of an ideal FET. The output conductance is zero and the transconductance is uniform to pinch-off. But such a device would eventually saturate at high power levels and show a sudden onset of distortion products simply because of clipping. The cases (a) and (b) are I-V characteristics of real FETs. These include two additional sources of nonlinearity which make their presence felt at lower power levels (than case c). These sources are the nonzero output conductivity G_d of the saturation characteristic and the fact that transconductance G_m ($= \Delta I/\Delta V_g$) varies considerably between the full current region ($V_g = 0$) and the neighborhood of pinch-off. The cases (a) and (b) provide a study of the effects of profile differences. (a) represents the I-V characteristics of an FET fabricated with a single deep implant (energy = 500 KeV Se^+) and (b) represents a case of lower energy implant of Se^+ in GaAs with the resulting profile being of higher carrier level near the surface. The difference in profiles causes considerable differences (in favor of the deep implant) in the sources of nonlinearity. It is this effect of carrier profile on device performance as measured by gain and the level of the third-order IMD product levels that shall be the focus of this discussion.

The equivalent circuit of Figure 2 is used to schematically represent the major distortion sources in an FET. The variation of G_m with V_g and the variation of G_d with V_d provide the main contribution of IMD. However, in Figure 2, two secondary sources of IMD are shown. They are the variation of C_{gs} with V_g and the variation of C_d with V_d. It is worth mentioning that C_d variations can cause detuning and gain expansion effects. These interesting phenomena must remain outside the scope of this discussion for the sake of brevity. Figure 2 shows the device embedded in a tuned amplifier configuration. In this analysis, it is assumed that the tuning is such that the load presented to the drain terminal is purely conductive.

Models of Nonlinearity

The main contributors to IMD, the transconductance G_m and the output conductance G_d must be described in a mathematical form that faithfully reproduces their effects in the calculation of IMD levels. The descriptions are polynomials where the coefficients contain all the relevant information. For example, for transconductance G_m:

$$G_m = G_{m1} + G_{m2} V_g + G_{m3} V_g^2 + G_{m4} V_g^3 + G_{m5} V_g^4 \ldots (1)$$

is a full description of the variation of transconductance as an instantaneous function of gate voltage V_g between $V_g = 0$ and $V_g = V_p$. V_p is the point of gate voltage range at which the device is carrying less than 5% of its I_{dss}.

For the drain output conductance there is a similar description:

$$G_d = G_{d1} + G_{d2} V_d + G_{d3} V_d^2 + G_{d4} V_d^3 + G_{d5} V_d^4 \ldots (2)$$

The coefficients G_{dn} contain a description of the variations of output conductance as an instantaneous function of drain voltage level. The drain coefficients are greatly reduced if the drain voltage level is raised so that the instantaneous drain voltage never approaches the saturation drain voltage. This corresponds to the commonly observed effect that low to medium power IMD levels are reduced by raising the drain bias voltage. The coefficients of both G_m and G_d are dependent

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upon the carrier profiles of the GaAs active layer. This dependence has been the reason for investigating different profiles both in theory and in practice to see how the level of IMD is controlled. In theory, the coefficients are derived from a detailed analysis of profile effects on device characteristics.

Carrier Profile Modeling

Practically all modeling of GaAs FETs has used analytical expressions derived from Shockley's[3] early work. Pucel et. al.,[4] in a more recent model, have included the effects of velocity saturation. These analyses of FET devices depended upon the assumption of a flat profile of a certain thickness for purposes of simplification, particularly of some of the integrals involved. To achieve the ability to deal with arbitrary profiles, numerical integration techniques have been added in what is an adaption of the Pucel model.

Figure 3 represents the model used to calculate the effects of nonflat profiles. This model may be used for the examination of flat profiles also, and has been for this discussion. The model deals with an arbitrary profile by dividing up the thickness of the active layer into as many as 150 laminar layers. The passage of an electron under the gate region is modeled as having a region of saturated velocity following the initial short section where velocity is proportional to electric field. By observing the necessary boundary conditions in the directions along and normal to the charge flow current may be established as a function of bias conditions. Also, gate capacitance and transconductance and output conductance may be calculated over any range of bias conditions.

The computer is programmed, therefore, to accept an analytical description of an active layer profile and to provide data on devices of specified geometry. The polynomial coefficients describing G_m and G_d over specified ranges of bias V_g and V_d are obtained from the computer. The effects of parasitic resistances, device geometry and various other phenomena may also be derived from this model.

Comparison of Profiles

The three profiles in Figure 4 have been used to examine the effect of profile tailoring on the nonlinear coefficients. A flat profile typical of an epitaxial layer is compared with an optimized nonflat (for nonlinearity as suggested by Williams[5]) epitaxial layer and with an ion implanted layer. The ion implanted layer in this case is "counter doped" by the additional implantation near the surface of an acceptor to deliberately distort the resulting profile.

The computer model was used to derive the G_m and G_d polynomial coefficients for these three profiles. These are shown in Tables 1 and 2. It is important to note that the magnitudes of the fifth-order coefficients is least for the ion implanted profile promising a better high power IMD performance. It is also noteworthy that in the case of transconductance, G_{m5} is larger than the G_{m3} for the flat profile device. The devices modeled for this comparison were 500 μm wide gates of 1 μm length with ohmic contact resistance of 10^{-6} ohm-cm^2.

IMD Calculation

The calculated IMD is based upon the normal two-tone-of-equal-power test. The procedure is straightforward but some very important points must be emphasized. Only third-order product has been calculated. Normally, it is assumed that the third-order coefficient (G_{m3} for instance) is much larger than the fifth or seventh (G_{m5}, G_{m7}). From Table 1 this is evidently not so. From an expansion of the higher order terms in Eqs. (1) or (2), it is seen that fifth-order coefficients do contribute substantially to third-order IMD products. In fact, for moderate to high signal levels the transconductance contributes mainly from its fifth-order coefficient term. This is seen from Table 3 where the contributions to each IMD product from the various coefficients are tabulated. This is the basic cause of the phenomena of "non well behaved IMD products" described by Strid and Duder.[6]

The second point to be made is that in the low power signal region, the IMD contributions of the drain conductance G_d dominate, and, as the signal level rises, the G_m contributions to IMD products become larger. There may be a correlation effect between these IMD products from the gate (G_m) and drain (G_d) giving rise to a cancellation effect at some intermediate signal level causing a sharp dip in an IMD product as a function of level. This is commonly observed.

Finally the sign of the fifth-order coefficient relative to the third-order coefficient may be quite important in determining the low signal level IMD products. In fact, cancellation can occur in third-order IMD products from the drain (or gate) alone due to sign differences of the different coefficients.

Profile Effects on IMD

In Figure 5 the outcome of the use of the coefficients of Tables 1 and 2 in calculation of IMD for the three different profiles is seen.

It is observed that the gain at small signal levels of both epitaxial devices is greater by about 1 dB. This calculation is for a 10 GHz test where the signals (two tones) are separated by only a few MHz. The gain of the ion implanted devices is less but decays less rapidly at saturation.

The IMD products have roughly three regions. At very low signal level, the third-order products rise 3 dB for a 1 dB increase in signal level. This is because the drain conductance G_d dominates here and because G_{d3} is sufficiently larger than G_{d5}. Then comes the middle signal level where the cancellation effects are generally seen. Sometimes quite sharp dips are seen in this region and a representation of this has been plotted in by a dotted line. In the large signal region, generally the contribution from transconductance G_m dominates and the rate of rise of the IMD product is greater than third-order. This is because G_{m5} may equal or exceed G_{m3}. Ion implantation displays a considerable advantage in this area because, for that case, G_{m5} is much less than G_{m3} and lower than equivalent values in other profiles. This results in the IMD product for the ion implanted FET continuing to have lower IMD products to higher power levels before complete saturation occurs.

Practical Comparison

The theory developed here represents a brief overview of the major factors involved in IMD distortion. Nevertheless, it has been subjected to a practical test. FETs fabricated from epitaxial wafers with uniform channnel doping (flat profile) have been compared with FETs fabricated using the ion implant prescription described in this discussion. The results are shown in Figure 6. It is seen that the results conform quite closely to the predictions of the simple theory and indicate an improved IMD performance from profile tailoring.

Conclusions

The main conclusion to come from this work is that a profile similar to the optimized epitaxial or the ion implanted profile provides better power FET performance through improved IMD performance. At the sacrifice of a small amount of gain level only at low signal level where it is relatively unimportant, an optimized ion implant profile is considered an excellent choice for high power level FET devices. A better understanding of the sources of IMD products emerges from this analysis.

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TABLE 1
POLYNOMIAL COEFFICIENTS OF $G_m(V)$

$$G_m = G_{m1} + G_{m2} V_g + G_{m3} V_g^2 + G_{m4} V_g^3 \cdots$$

Coefficient	Flat Epi	Optimized Epi	Ion Implant $Se^+ + Be^+$
G_{m1}	.035	.0355	.031
G_{m2}	.0058	.004	.0033
G_{m3}	-.00045	-.0007	.00075
G_{m4}	.00033	.00058	-.000054
G_{m5}	.00146	.0009	-.0002
G_{m6}	.00005	-.0001	.000042
G_{m7}	-.0002	-.0001	.0000448
G_{m8}	.000005	.000015	-.0000047

TABLE 2
POLYNOMIAL COEFFICIENTS OF $G_d(V)$

where $G_d = G_{d1} + G_{d2} Vd + G_{d3} Vd^2 + G_{d4} Vd^3 + G_{d5} Vd^4 \ldots$

Coefficient	Flat Epi	Optimized Epi	Ion Implant $Se^+ + Be^+$
G_{d1}	1.64 E-4	1.99 E-4	4.28 E-4
G_{d2}	-3.07 E-5	-4.19 E-5	-4.90 E-5
G_{d3}	1.134 E-5	5.18 E-6	-2.23 E-6
G_{d4}	-1.37 E-6	7.62 E-7	1.23 E-7
G_{d5}	-3.92 E-7	-2.25 E-7	1.26 E-7
G_{d6}	5.80 E-8	-8.47 E-9	-2.02 E-8
G_{d7}	6.20 E-9	5.4 E-9	2.00 E-9
G_{d8}	-8.21 E-10	-3.41 E-10	-1.08 E-10

TABLE 3
TWO TONE TEST INTERMODULATION PRODUCTS

$$V = A \cos 2\pi f_1 t + B \cos 2\pi f_2 t$$

IMD Source	Third $2f_1 - f_2$	Fifth $3f_1 - 2f_2$	Seventh $4f_1 - 3f_2$	Ninth $5f_1 - 4f_2$
$(G_3x)\ V^3$	$.75A^2B$			
$(G_5x)\ V^5$	$1.25A^4B$ $1.875A^2B^3$	$.625A^3B^2$		
$(G_7x)\ V^7$	$1.64A^6B$ $6.56A^4B^3$ $3.28A^2B^5$	$1.64A^5B^2$ $2.187A^3B^4$	$.547A^4B^3$	
$(G_9x)\ V^9$	$1.97A^8B$ $14.76A^6B^3$ $19.687A^4B^5$ $4.92A^2B^7$	$2.95A^7B^2$ $9.84A^5B^4$ $4.92A^3B^6$	$1.969A^6B^3$ $2.46A^4B^5$	$.49A^5B^4$

i.e., for $G_3 \neq 0 \quad G_5 \neq 0 \quad G_{n\ 5} = 0$

$$I_{2f_1-f_2} = .75\ G_{m3}A^2B + 1.25\ G_{m5}A^4B + 1.875\ G_{m5}A^2B^3$$

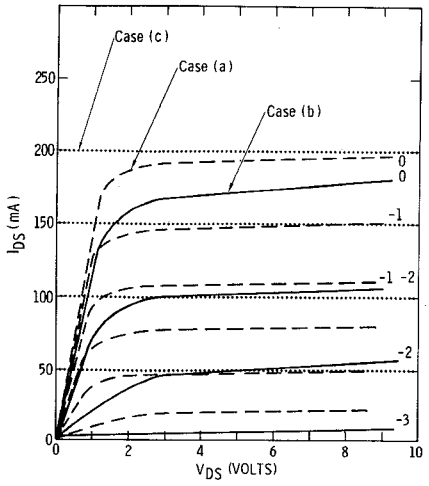

Fig. 1 Current-voltage characteristics of ion implanted GaAs FET devices. Case (a) Se^+ implant $3x10^{12}$ at 500 keV. Case (b) Se^+ implant $4x10^{12}$ at 200 keV. Case (c) represents the ideal FET.

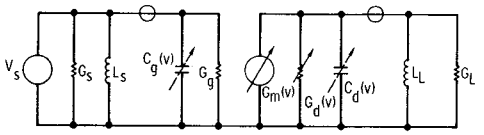

Fig. 2 Equivalent circuit of power FET and tuned source and load. The primary and secondary sources of non linearity are indicated.

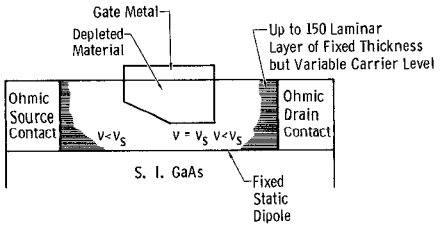

Fig. 3 Laminar layer models used in the modeling of GaAs FETs with variable carrier concentration profiles.

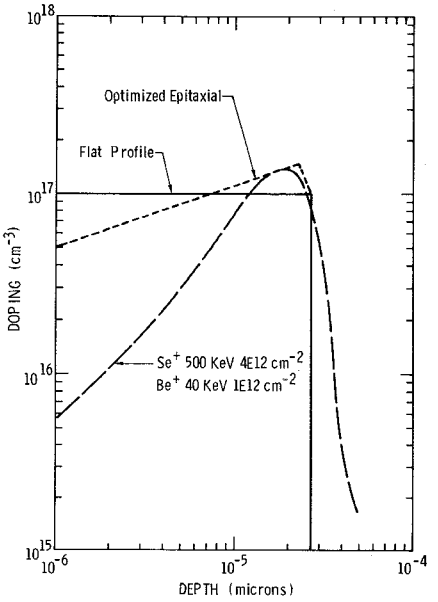

Fig. 4 The profiles used for a theoretical comparison of the IMD behavior of FETs.

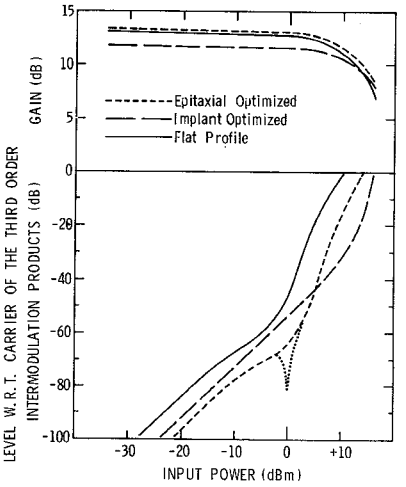

Fig. 5 Calculated values of gain and IMD level for similar FETs fabricated from the profiles of Fig. 4.

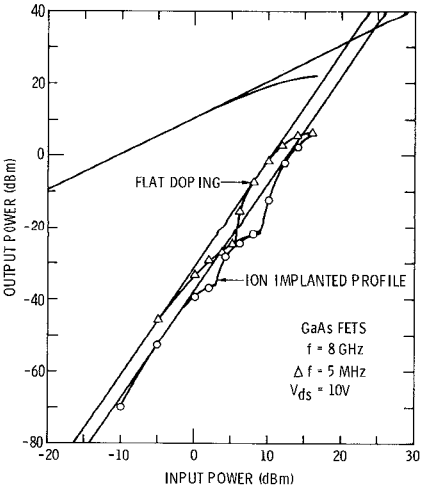

Fig. 6 Measured values of output power level and IMD level in an experimental comparison of profiles.